Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) In a processor, a method for performing computer graphics view volume clipping comparisons to determine [[if]] whether a vertex is located within a specified view volume, the method comprising:

transforming ~~a plurality of~~ coordinates representing the vertex into ~~a plurality of~~ transformed coordinates; and

using a floating point magnitude compare instruction to

~~determine an absolute value of at least one of the plurality of transformed coordinates and an absolute value that represents, for each respective at least one transformed coordinate, opposing view volume edges in the specified view volume in a dimension corresponding to the respective at least one transformed coordinate, and~~

perform a magnitude comparison between [[the]] an absolute value of [[the]] at least [[one]] two of the ~~plurality of~~ transformed coordinates and [[the]] an absolute value of [[the]] a corresponding view volume [[edges]] edge, wherein comparison results indicate whether the at least two of the transformed coordinates are within the ~~for at least two~~ view volume ~~edges are obtained~~.

2. (Canceled).

3. (Previously Presented) The method of Claim 1, further comprising:

setting a plurality of condition code bits to one or more specific states to indicate results of the magnitude comparison.

4. (Previously Presented) The method of Claim 1, further comprising:

specifying a compare condition in the floating point magnitude compare instruction.

5. (Previously Presented) The method of Claim 4, further comprising:

setting one of the plurality of condition code bits to indicate true if an associated compare condition is true and setting the one condition code bit to indicate false if the associated compare condition is false.

6. (Previously Presented) The method of Claim 1, further comprising:

converting a plurality of fixed point values into a plurality of floating point values using a first convert instruction.

7. (Previously Presented) The method of Claim 6, wherein the first convert instruction is a CVT.PS.PW instruction.

8. (Previously Presented) The method of Claim 6, further comprising:

converting a plurality of floating point values into a plurality of fixed point values using a second convert instruction.

9. (Previously Presented) The method of Claim 8, wherein the second convert instruction is a CVT.PW.PS instruction.

10. (Previously Presented) The method of Claim 1, wherein the floating point magnitude compare instruction is a CABS instruction.

11. (Currently Amended) A system that performs computer graphics view volume clipping comparisons to determine [[if]] whether a vertex is located within a specified view volume, the system comprising:

means for transforming ~~a plurality of~~ coordinates representing the vertex into a plurality of transformed coordinates; and

means for executing a floating point magnitude compare instruction to ~~determine an absolute value of at least one of the plurality of transformed coordinates and an absolute value that represents, for each respective at least one transformed coordinate, opposing view volume edges in the specified view volume in a dimension corresponding to the respective at least one transformed coordinate, and~~

perform a magnitude comparison between [[the]] an absolute value of [[the]] at least [[one]] two of the ~~plurality of~~ transformed coordinates and [[the]] an absolute value of [[the]] a corresponding view volume [[edges]] edge, wherein comparison results indicate whether the at least two of the transformed coordinates are within the ~~for at least two~~ view volume ~~edges are obtained~~.

12. (Previously Presented) The system of Claim 11, further comprising:

means for setting a plurality of condition code bits to one or more specific states to indicate results of the magnitude comparison.

13. (Previously Presented) The system of Claim 11, further comprising:

means for specifying a compare condition in the magnitude compare instruction.

14. (Previously Presented) The system of Claim 13, further comprising:

means for setting one of the plurality of condition code bits to indicate true if an associated compare condition is true and setting the one condition code bit to indicate false if the associated compare condition is false.

15. (Previously Presented) The system of Claim 11, further comprising:

means for converting a plurality of fixed point values into a plurality of floating point values using a first convert instruction.

16. (Previously Presented) The system of Claim 15, wherein the first convert instruction is a CVT.PS.PW instruction.

17. (Previously Presented) The system of Claim 15, further comprising:

means for converting a plurality of floating point values into a plurality of fixed point values using a second convert instruction.

18. (Previously Presented) The system of Claim 17, wherein the second convert instruction is a CVT.PW.PS instruction.

19. (Previously Presented) The system of Claim 11, wherein the floating point magnitude compare instruction is a CABS instruction.

20-39. (Canceled)

40. (Currently Amended) The method of Claim 1, wherein the ~~plurality of~~ coordinates and the ~~plurality of~~ transformed coordinates are in a paired-single data format.

41. (Currently Amended) The system of Claim 11, wherein the ~~plurality of~~ coordinates and the ~~plurality of~~ transformed coordinates are in a paired-single data format.

42. (Previously Presented) The method of Claim 1, wherein the floating point magnitude compare instruction is part of a general purpose instruction set architecture.

43. (Previously Presented) The method of Claim 1, wherein the floating point magnitude compare instruction is part of an application specific extension to a general purpose instruction set architecture.

44. (Previously Presented) The method of Claim 1, wherein the floating point magnitude compare instruction is executed in a single clock cycle.

45. (Canceled).

46. (Previously Presented) The system of Claim 11, wherein the floating point magnitude compare instruction is part of a general purpose instruction set architecture.

47. (Previously Presented) The system of Claim 11, wherein the floating point magnitude compare instruction is part of an application specific extension to a general purpose instruction set architecture.

48. (Previously Presented) The system of Claim 11, wherein the floating point magnitude compare instruction is executed in a single clock cycle.